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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/819,870	03/28/01	CORISIS	D 3770.305 C97

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MM92/0606

EXAMINER	
QUINTO,K	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/06/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/819,874	CORISIS ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other:

DETAILED ACTION

Claim Objections

1. Claim 7 is objected to because of the following informalities: the use of the term "alignment cut-out." The metes and bounds of the term "alignment cut-out" are unclear to the examiner. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-4, 6-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Liang (USPN 5,378,924).

4. In reference to claim 1, Liang (USPN 5,378,924) discloses an integrated circuit package. In figure 4 of Liang, there is a semiconductor die (11) which is conductively coupled to a plurality of conductors/leads (15). In figure 6, there is an alignment feature (74) in the lead frame (70) which is separate from the plurality of leads/conductors.

5. With regard to claim 2, Liang discloses (in figure 6) an alignment feature (74). This locating hole (74) is used for proper alignment in the mold cavity (column 5, lines 62-64). It is also an aperture.

6. Claim 3 states that the alignment feature is semi-circular shaped. The alignment feature (74) seen in figure 6 of Liang is formed of two semi-circular shaped holes.

7. Claim 4 states that an insulating material encompasses the semiconductor die and a portion of each of the plurality of leads/conductors. The insulating material has a first and second end which each have an alignment feature. In figure 4 of Liang, the molding cavity (40) is filled with an encapsulant or insulating material. It is understood that the insulating material encompasses the semiconductor die and a portion of each of the plurality of leads/conductors to make a finished integrated circuit package. As a result of the encapsulation procss, the insulating material also encompasses the alignment feature (74 of figure 6).

8. With regard to claim 6, Liang meets its limitations. In figure 4 of Liang, there is a semiconductor die (11) which is conductively coupled to a plurality of conductors/leads (15). In figure 6, there is an alignment feature (74) in the lead frame. This alignment feature, as stated above with regard to claim 4, is encompassed by an insulating material.

9. So far as understood, Liang meets the limitations of claim 7. The examiner interprets "alignment cut-out" to mean any opening in the lead frame or die-attach paddle which is aligned with the package. In this case, the alignment feature of Liang (74 in figure 6) meets this limitation.

10. With regard to claims 8 and 9, the alignment feature (74) seen in figure 6 of Liang is formed of two holes or apertures which are semi-circular shaped.

11. In reference to claim 10, the alignment feature of Liang (74) is on a tie bar (72).

12. Claim 11 states that the alignment feature is disposed on a first end and a second end of a lead frame. In figure 6, the alignment feature (74) is on a lead frame (70). It is understood that there are four of these alignment features (74) on the lead frame (70) in the same manner illustrated in figure 5 of Liang. In figure 5, the alignment features (68a-68d) are in four different positions on the lead frame (60). These alignment features (68a-68d) are on a first end and on a second end of the lead frame (60).

13. Claims 1, 4–6 are rejected under 35 U.S.C. 102(e) as being anticipated by Perino et al. (USPN 6,007,357).

14. In reference to claim 1, Perino et al. (USPN 6,007,357, hereinafter referred to as the "Perino" reference) discloses a similar integrated circuit package. In figure 19 of Perino, an integrated circuit package is illustrated. There is a chip (1900) with a plurality of conductors or leads (not numbered) on the bottom of the chip (1900). Although not shown, it is understood that there is a semiconductor die within the chip and furthermore it is conductively coupled to the plurality of leads. The chip (1900) also has an alignment feature in the form of a left arm (1901) and a right arm (1903) which are separate from the plurality of leads or conductors.

15. Claim 4 cites the limitation that an insulating material encompasses the semiconductor die and a portion of each of the plurality of conductors. It also states that the insulating material has a first and second end with an alignment feature disposed on both ends.

The device of Perino in figure 19 meets the limitations of claim 4. It is understood that the chip (1900) has an insulating material as its package. It is also understood that there is a semiconductor die (not seen) within the package which is conductively coupled to the plurality

of leads/conductors (not numbered in figure 19) on the bottom of the chip (1900). Figure 19 also illustrates that the insulating material encompasses a portion of each of the plurality of leads/conductors. Figure 19 shows that the insulating material has two ends, with an alignment feature in the form of a left arm (1901) and of a right arm (1903) on each end.

16. With regard to claim 5, the device of Perino discloses a protuberance as an alignment feature. In figure 19, the left arm (1901) and the right arm (1903) are each a protuberance.

17. In reference to claim 6, Perino discloses an integrated circuit package in figure 19 which meets the claim's limitations. It is understood that there is a semiconductor die within the chip package (1900). It is also understood that the die is conductively coupled to the plurality of conductors/leads visible on the bottom of the chip (1900). Figure 19 of Perino also shows an alignment feature in the form of a left arm (1901) and of a right arm (1903). One arm is on each end. An insulating material encompasses both arms.

18. Claims 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Kwon (USPN 5,369,550).

19. In reference to claim 6, Kwon (USPN 5,269,550) discloses an integrated circuit package in figures 2 and 3 which meets the claim's limitations. Figure 2 shows the integrated circuit package where there is a die (20) and a plurality of leads/conductors (24 and 26) which are conductively coupled to the die (20). There is a hole or aperture (14 in figure 2, 15 and 50 in figure 3) in the die-attach paddle (22 in figures 2 and 3) which is aligned with a hole in the package. The package or insulating material encompasses it.

20. So far as understood, Kwon meets the limitations of claim 7. The examiner interprets "alignment cut-out" to mean any opening in the lead frame or die-attach paddle which is aligned

with the package. There is a hole or aperture (14 in figure 2, 15 and 50 in figure 3) in the die-attach paddle (22 in figures 2 and 3) which is aligned with a hole in the package. The examiner interprets the hole or aperture (14 in figure 2, 15 and 50 in figure 3) to be an "alignment cut-out."

21. With regard to claim 8, the alignment feature is indeed a hole or aperture (14 in figure 2, 15 and 50 in figure 3) in the die-attach paddle (22 in figures 2 and 3).

22. Claims 6, 10, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Przano (USPN 5,714,792).

23. With regard to claim 6, Przano discloses an integrated circuit package in figure 1 which meets the claim's limitations. Figure 1 shows an integrated circuit package with a semiconductor die (11) which is conductively coupled to a plurality of leads/conductors (16). In paragraph [0036] on p.8-9 of the specification, the applicant has defined an alignment portion to include a tie bar and other parts of the lead frame which provide internal support to the integrated circuit package. Figure 1 of Przano shows an alignment feature in the form of a tie bar (20), which is a part of the lead frame (13). It is understood that a plastic package or insulating material will encompass it in the course of fabrication.

24. In reference to claim 10, the alignment feature of Przano in figure 1 is a tie bar (20) as stated above.

25. Claim 11 states that the alignment feature is on both ends of a lead frame. In figure 1 of Przano, there are two tie bars (20) on the lead frame; one on each end.

26. Claim 12 states that the alignment feature is a protuberance. In figure 1 of Przano, the two tie bars (20) are protuberances from the lead frame.

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perino et al. (USPN 6,007,357) in view of Montgomery (USPN 3,882,807).

29. In reference to claim 13, Perino does not disclose that a lead frame is a part of mass produced strip of lead frames and is separated from the strip. Perino inherently meets the other limitations of claim 13. It is understood that there is a semiconductor die within the chip package (1900). It is also understood that the die is conductively coupled to the plurality of conductors/leads visible on the bottom of the chip (1900). An insulating material encompasses both the die and portions of the plurality leads/conductors. Figure 19 of Perino also shows an alignment feature in the form of a left arm (1901) and of a right arm (1903). One arm is on each end. Since these arms are made of the insulating material, they are indeed electrically isolated from the plurality of leads/conductors.

It is well-known in the art that one lead frame is part of a mass produced strip of lead frames and is separated from that strip. This can be seen in figure 1a of Montgomery where there are two lead frames (10 and 12) that are cut along the shear line (16). Lead frames are mass produced in strip-form and are ready for cutting so as to facilitate large scale production of integrated circuit chips. One would be motivated to use the strip form of lead frames in the

device of Perino so as to facilitate its mass production. Therefore it would be obvious to use lead frames in strip-form and are ready for cutting in the device of Perino.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
June 4, 2001

Nathan Flynn
Primary Examiner